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Ph.D. THESIS SUMMARY

Eng. Anca Mihaela DRĂGAN (VASILE)

CIRCUITE INTEGRATE DE JOASĂ PUTERE PENTRU SENZORI

INTEGRATED CIRCUITS WITH LOW POWER FOR SENSORS

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Content

Chapter 1

Introduction

1.1 Presentation of the field of the doctoral thesis

The new latest trends in the sensor market reveal a 15% increase in sales for temperature sensors (TS), owning to their high demand across multiple use cases, including medical applications, industrial processes, automotive, and electronic consumers. General-purpose electronics like PCs, laptops and smartphones require high-speed memory modules with increased efficiency. The preferred choice for such applications is the digital temperature sensor with integrated serial interface (DTS). The sensor monitors the temperature on chip and generates an alert signal if a failure is detected.

This PhD paper focuses on presenting a digital thermal detector with a serial interface designed for DIMM modules (Dual In Line Memory Modules) following the DDR4 (Double Data Rate 4^{th} Generation) JEDEC standard.

1.2 Scope of the doctoral thesis

The primary focus of this doctoral thesis is the design of a digital temperature sensor featuring an integrated serial interface. The functionality and performances of the integrated sensor will be thoroughly investigated through simulations. This sensor will be SI implemented and its validation will be conducted through measurements and characterizations of various encapsulated structures.

To achieve optimal competitiveness in the digital temperature sensor market, the following stringent requirements are set:

- Low power supply voltages.
- High accuracies.
- Wide range of detected temperatures.
- Minimal area consumption.
- Low current consumption.
- High frequencies for digital communication.
- Serial interfaces that are compatible with the chosen application.

1.3 Content of the doctoral thesis

The PhD thesis is organized into four parts. The first part provides a brief overview of the principal types of temperature sensors and their typical applications. The second part introduces the standard architecture of a digital temperature sensor. To address the stringent requirements imposed to the DTS's market, this section will detail the limitations and the constrains associated with the standard topology of the investigated sensor. In the third part, innovative solutions that enhance the performances of the standard topology will be presented. New low-power blocks are proposed for the integrated sensor to meet the specified requirements, and these blocks will be thoroughly analyzed through simulations and experimental results. The final part of the thesis will unveil the new architecture of the temperature sensor incorporating all the improved blocks. The performances of the sensor will be comprehensively analyzed through simulations, wafer measurements and characterization of encapsulated chips.

The second chapter initiates with the classification of the most sought-after temperature sensors. Each type of sensor will undergo analyzed based on functionality, temperature characteristics, readout circuits and primary applications. The study further includes the presentation of the specific parameters, accompanied by a brief performance comparison. This comparison aims to highlight the significance of each sensor type within tis respective application context. A focus will be placed on the digital sensors due to their widespread utility in DIMM memory modules, medical applications, and the automotive field.

The third chapter introduces the structure of a DTS, comprising the sensor itself, which detects temperature, a digital control circuit and a serial interface. The sensor itself consists of a block that detects temperature through an analog voltage proportional to the sensed temperature and an analog-to-digital converter that transforms the analog voltage into a digital format. The digital control circuit processes the binary temperature data and transmits it to the serial interface. Additionally, the control circuit is responsible for generating an alert signal if the detected temperature exceeds predefined threshold limits. The serial interface facilitates communication between the sensor itself and a microcontroller. This chapter provides a detailed analysis of each circuit within the standard architecture of the sensor. Furthermore, it discusses the drawbacks associated with the classical topology:

- Analog circuits must maintain constant voltages and currents over time to ensure accurate interpretation of the digital temperature.
- Digital output circuits in the standard implementation typically operate at low frequencies and high-power supply voltages.
- There is a need for a trimming block to minimize temperature error of the sensor.

The fourth chapter focuses on the auto-zero circuit used in the reference voltage block, which is part of the sensor itself. Simulated results of the reference reveal a significant drift over time, especially notable at high temperatures and low power voltages. This drift becomes more pronounced with an extended investigation time interval. The drift in time of the sensor has a substantial impact on the analog voltages, potentially leading to inaccurate temperature readings. This chapter proposed a new architecture for the autozero circuit aimed at eliminating the drift over time observed in the classical topology.

In the fifth chapter, a new architecture of digital output buffers for DTS will be presented. The evolving requirements of sensors with digital interfaces demand high operating frequencies and low-power voltages for effective communication with a microcontroller. The chapter introduces two new digital output circuits:

- A push-pull output buffer is proposed for I^2C Ultra-Fast Mode and SPI interfaces,
- An open-drain output buffer is proposed for I^2C High Speed interface.

These circuits, designed for high-speed frequencies at low power voltages are validated by simulations and measurements. The experimental data highlights the superiority of the open-drain circuit for the I^2C High Speed interface.

The sixth chapter encompasses the new architecture of the sensor, incorporating the innovative solutions presented in the fourth and fifth chapters. The performance of the DTS with respect to accuracy is thoroughly investigated across the entire sensed temperature domain. In plus, a trimming circuit with EEPROM memories is proposed for adjust the temperature error of the integrated system. The digital temperature sensor equipped with the I^2C High Speed interface and EEPROM trimming circuit is SI implemented. To investigate the temperature error of the sensor, 25 encapsulated circuits are measured.

In the conclusion chapter, the obtained results presented in this paper will be comprehensively considered. The original contributions, the list of scientific published papers and the further research directions will be presented.

Chapter 2

Temperature sensors and read-out circuits

2.1 Types of temperature sensors

A temperature sensor is an integrated circuit that detects temperature and transmits it through physical quantity dependent on the detected temperature [1] [2] [3]. There are several families of temperature sensors: resistive sensors and electronic sensors. Resistive sensors have a resistance thermosensitive element with a positive coefficient (PTC) and with negative coefficient (NTC). The electronic sensors are circuits classified by their read-out circuit into analog sensors (ATS) and digital sensors (DTS). Modern trends highlight the use of the digital temperature sensors with integrated interfaces for DIMM [4]. These sensors play a crucial rule in monitoring the temperature of memory modules. Due to their integration with a serial interface, DTS can communicate with a microcontroller (CPU).

2.2 DTS Parameters

In this paper, a new architecture of digital temperature sensors is proposed. This section focuses on presenting the parameters relevant to DTS. Almost every parameter discussed here is universally applicable to various temperature sensors. **Table.2.1** compares three DTS products - N34TS00, N34TS04 and TMP1075 - based on their specific parameters.

Table 2.1 *Performances of three DTS products*

Parameter	Limit Value	Product
Temperature Range	-20…125℃	N34TS00/04
	-55…125℃	TMP1075
Power supply voltage	2.2…5.5V	N34TS04
	1.6 …5.5V	TMP1075
	1.7…1.9V	N34TS00
Temperature Error	±3℃ (-20…125℃)	N34TS00/04
	±2℃ (-55…125℃)	TMP1075
Current consumption	1000 µA (-20…125℃)	N34TS04
	15 µA (-40…125℃)	TMP1075
	0.001…1MHz –Fast +	N34TS04
	0.001…3.4MHz –High Speed	TMP1075

Chapter 3

Digital temperature sensor with I^2C interface (DTS I^2C)

3.1 Block Schematic. Functionality

The digital temperature sensor is an integrated circuit that measures the temperature and monitors the thermal performances of a digital system [5]. The circuit detects the temperature,

converts it in a digital format, and if the temperature exceeds the optimal threshold limits, an alert signal is asserted, leading to the deactivation of the entire system [6].

The sensor with the serial interface I^2C (DTS I^2C) consists of two pins for facilitating digital communication: an input pin for the serial clock line (SCL) and a bidirectional pin for the serial data line (SDA). The SCL signal establishes the operating frequency for digital communication, while SDA manage the exchange of information between the sensor and the digital system. Additionally, the detector includes a power supply pin V_{DD}, a ground pin GND and an output pin ALERT, used to deactivate the entire digital system when necessary.

The block schematic of the DTS I^2C (**Fig.3.1**) comprises the DTS sensor itself, a digital control circuit and an I^2C interface. The sensor converts the sensed temperature into a digital signal TEMP. The binary temperature is then transmitted to the control circuit, which compares the temperature with the optimal threshold values. The interface facilitates communication between the sensor and a CPU by transmitting the sensed temperature on the serial data line.

3.2 DTS Circuit

The DTS circuit (**Fig.3.1**) consists of a reference voltage block and an analog-to-digital converter [7] [8] [9] [10]. The reference provides a constant output voltage (V_{REF}). Also, the circuit contains the thermosensitive element of the sensor (two PNP BJT devices) and generates a Proportional to Absolute Temperature (PTAT) current (I_{PTAT}) [11]. V_{REF}, I_{REF} and I_{PTAT} are used for converting the temperature into a digital format [12]. The ADC block compares the difference of the analog currents (I_{REF}, I_{PTAT}) with V_{REF} and outputs a signal represented by 12 bits (TEMP).

3.3 Digital Control Circuit (CTRL DIG)

The digital control circuit (**Fig.3.1**) is responsible for monitoring the thermal performances of the sensor. The blocks within this circuit include temperature registers for storing information related to the detected temperature (TEMP), the maximum threshold (TEMP_MAX) and minimum temperature (TEMP_MIN). Additionally, there is an alert monitoring block and a digital output buffer. The alert monitoring block compares these threshold values with the sensed temperature and generates an alert signal if a failure is observed.

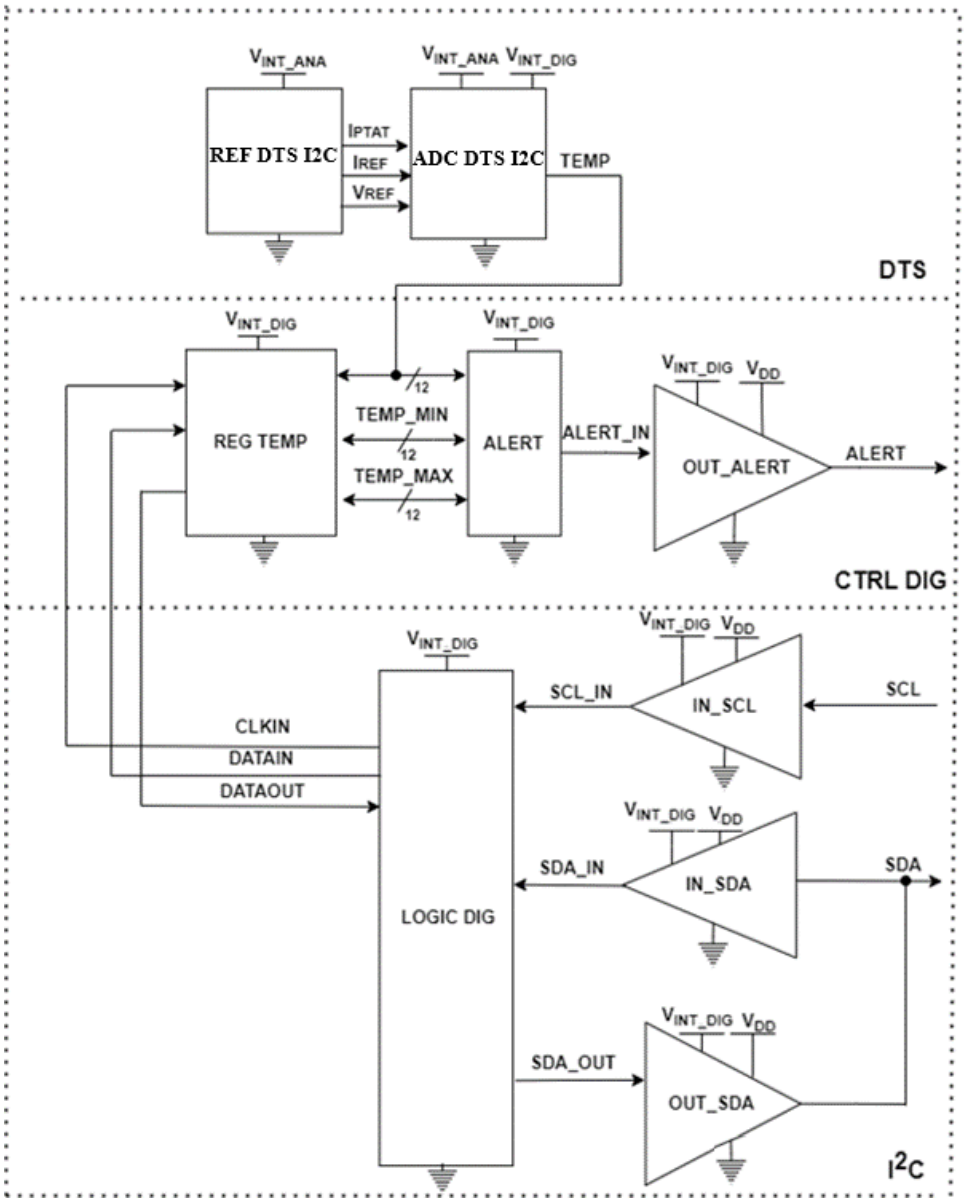


Fig. 3.1 *Block Schematic of DTS I²C*

3.4 I²C Serial Interface

The memory module and the sensor communicate through a digital interface via serial data and clock transmissions (**Fig.3.1**) [13] [14]. The I²C interface employs a communication protocol that allows multiples operation modes, with most of them utilizing an open-drain digital output buffer for data transmission. Standard, Fast, Fast+ and High Speed I²C modes are used. The fastest interface is High Speed I²C and operates up to 3.4MHz.

In addition to open drain buffers, push-pull buffers are used for data transmission through the 2-wired interface for I²C UFm (Ultra-FastMode), enabling operating frequencies up to 5MHz [15]. Other high-speed interfaces utilizing push-pull digital output buffer include SPI (10MHz) and I³C (12.5MHz).

Chapter 4

Autozero circuits for DTS I²C in a CMOS EEPROM process

4.1 DTS I²C reference voltage

The reference voltage block of the DTS sensor (REF DTS I²C) is illustrated in **Fig.4.1**. The circuit contains several autozero blocks (AZ) designed to eliminate the offset. The reference itself is implemented in a 0.18µm CMOS EEPROM with LV(Low-Voltage) devices. To monitor the reference voltage output during test, an autozero block implemented with HV devices is used (TEST REF DTS I²C).

A consistent drift in the reference voltage (V_{REF}) over time (conversion time is approx. 200ms) was observed during HSPICE simulations leading to inaccurate temperature readings. The responsible blocks for the unwanted drift over time are the autozero circuits. As a result, further investigation into the architecture of the autozero with the DTS I2C voltage reference is necessary.

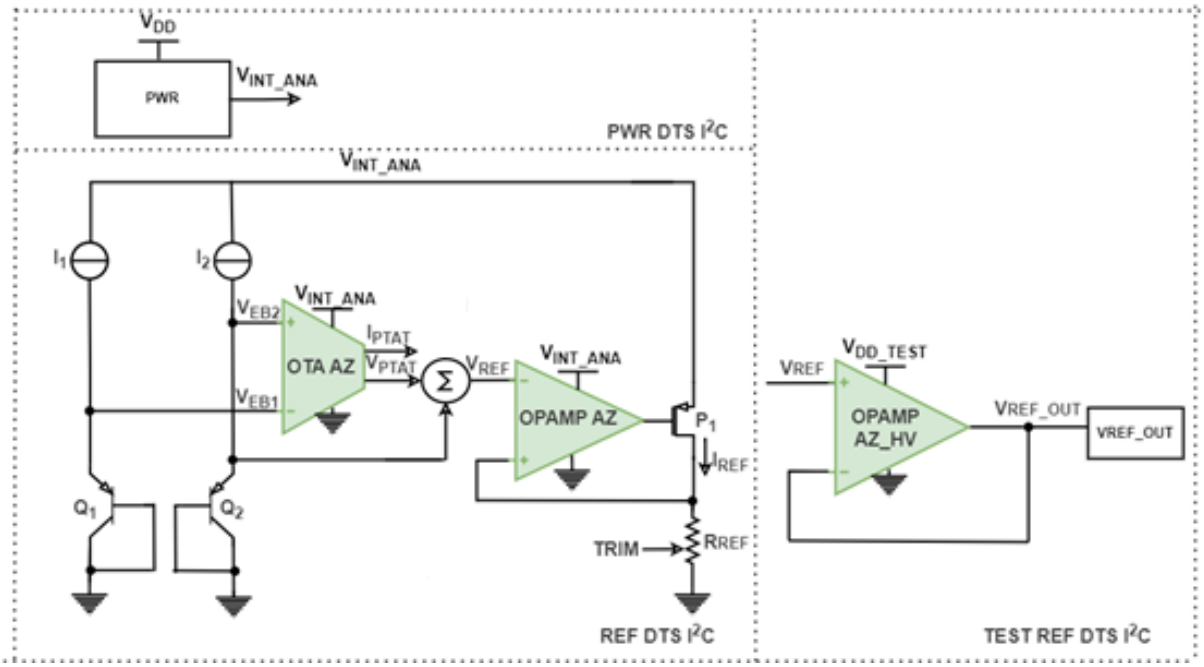


Fig. 4.1 *DTS I²C reference voltage*

4.2 The standard architecture of the autozero circuit

The block schematic of the autozero circuit is depicted in **Fig.4.2**. In the case of DTS I^2C, the autozero technique involves applying a finite number of pulses to the switches S_1 – S_5. This process eliminates the offset of the principal amplifier (Gm). After offset elimination, the feedback path formed by the output stage (R) and the secondary amplifier (Gm') is deactivated. The comportment in time of the output voltage of the autozero circuit (V_{OUT}) in relation to the input voltage of the Gm' (V_{INM}', V_{INP}') are illustrated in **Fig.4.3**.

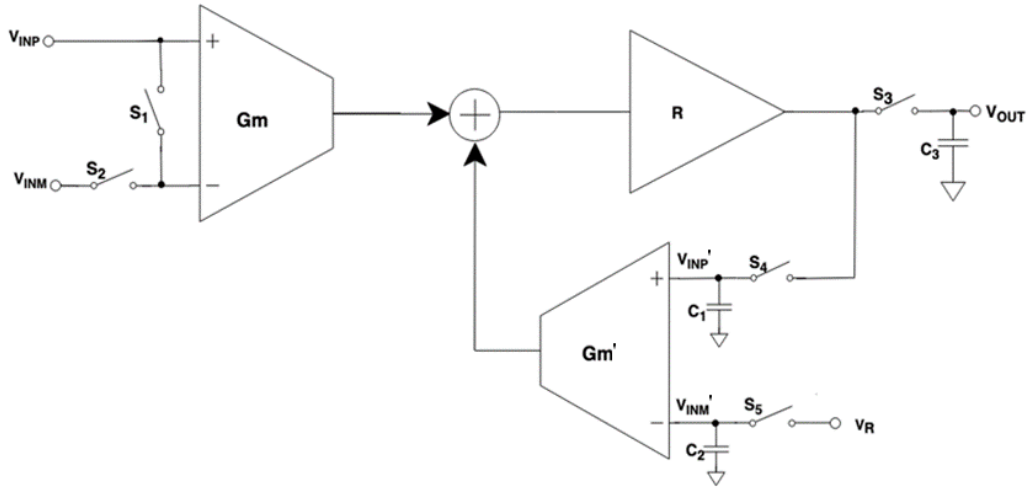


Fig. 4.2 *Standard autozero circuit – Block Schematic*

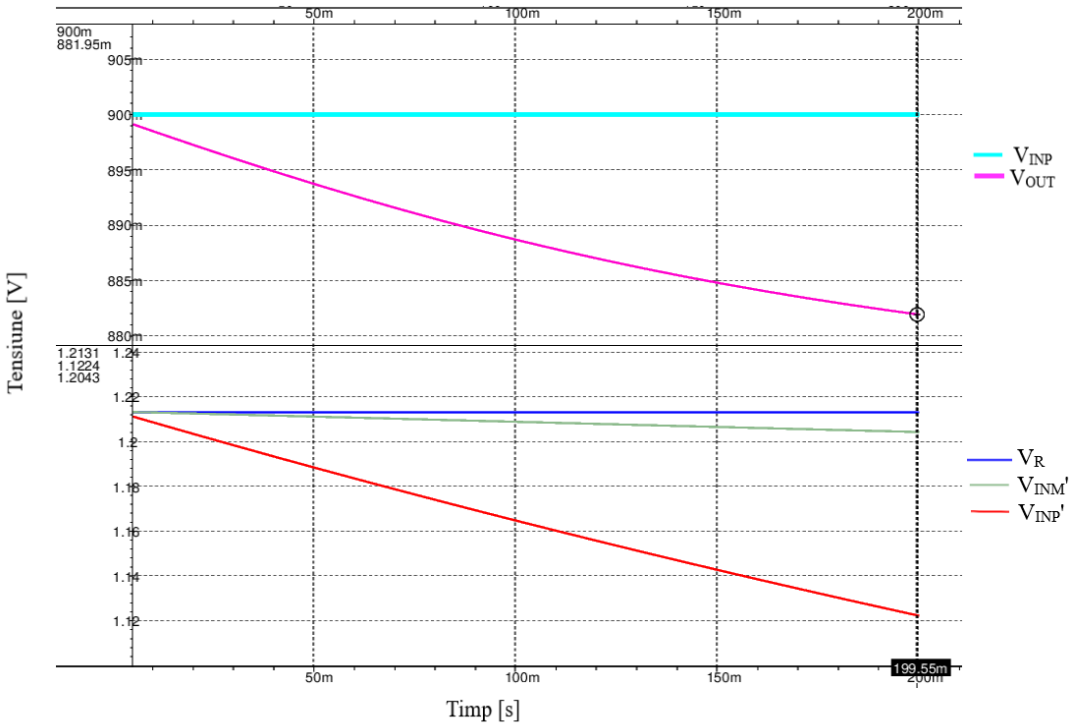


Fig. 4.3 *The behavior of the standard autozero circuit in 200ms at 25°C*

4.3 The improved autozero architecture

The improved architecture of the autozero circuit is shown in **Fig.4.4**. The proposed circuit includes several new switches: S_6, S_7, S_8, S_9, which ensure same potentials across the input of the secondary amplifier (Gm') [16]. The symmetrical configuration formed by S_8 and S_9 assures same potentials on a terminal of the switches S_4, S_5. Also, same voltages across S_6 and S_7 permits equal voltages on the inputs of the secondary amplifier. The behavior in time of the output voltage of the improved autozero block (V_{OUT}), and the input voltages of Gm' (V_{INM}', V_{INP}') is figured in **Fig.4.5**.

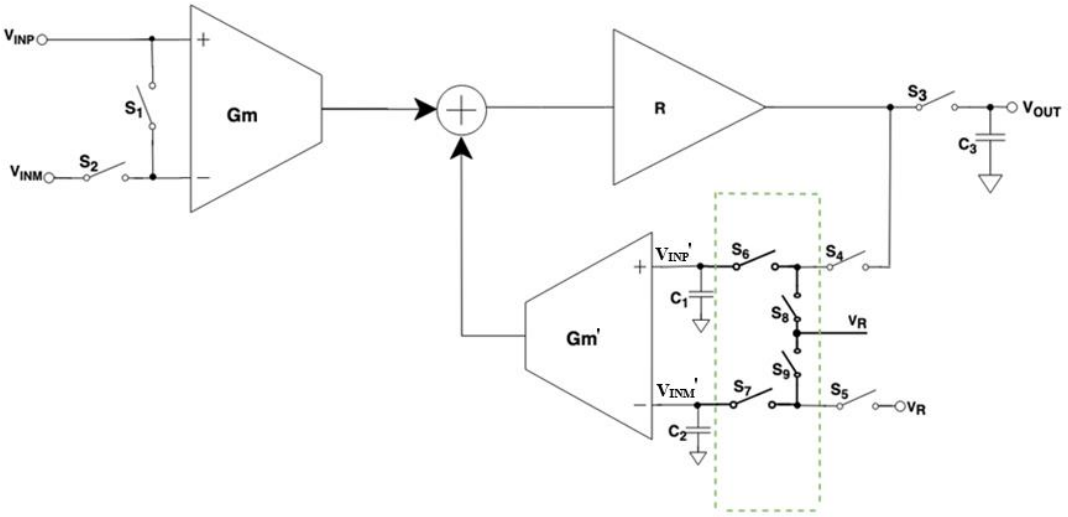


Fig. 4.4 *Improved autozero circuit – Block Schematic*

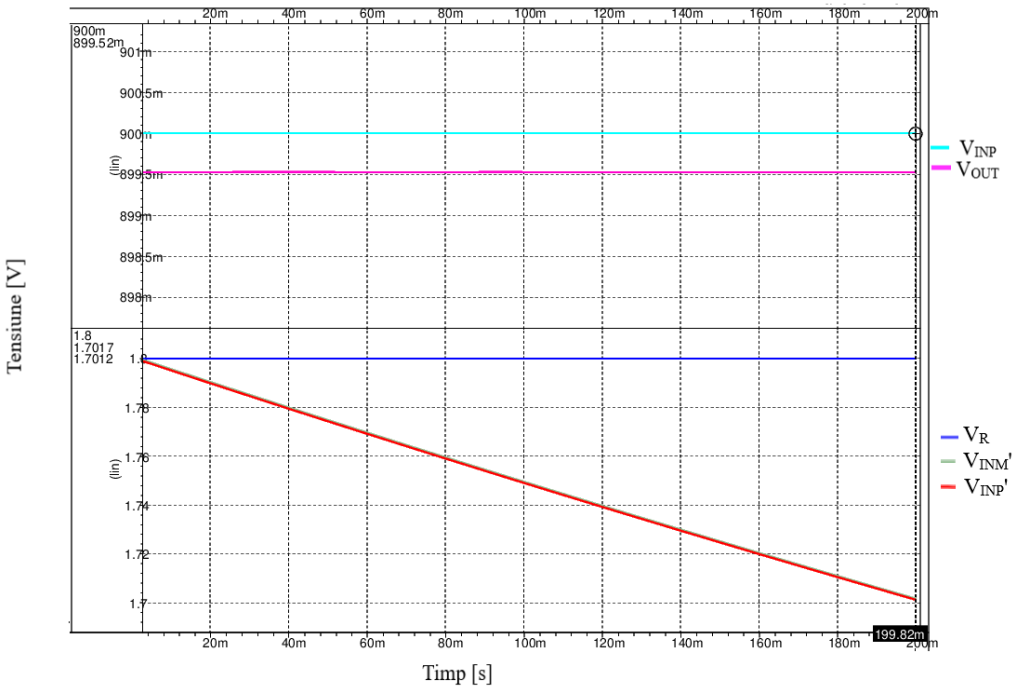


Fig. 4.5 *The behavior of the improved autozero circuit in 200ms at 25°C*

4.4 The comparison of the standard and the improved auto-zero circuits

The autozero circuits implemented with HV devices (**Fig.4.2, 4.4**) were compared using HSPICE PVT simulations. In **Fig.4.3** a drift of 20mV for V_{OUT} can be observed during the analyzed time. This drift is more pronounced at higher temperatures and lower power supply voltages. The drift over time of V_{OUT} is attributed to different potentials on the inputs of Gm' stage. **Fig.4.5** confirms the equilibrium of the V_{INP}', V_{INM}' potentials and the elimination of the drift over time for V_{OUT} with the improved architecture (**Fig.4.4)**. Also, Monte Carlo simulations was considered. All investigated scenarios showed the elimination of the drift in time at the output of the improved circuit (**Fig.4.4**).

4.5 The comparison of REF DTS I^{2}C with the standard and the improved autozero circuits

The voltage reference block (**Fig.4.1**) with the standard autozero circuits (**Fig.4.2**) and REF DTS I^{2}C with the proposed AZ circuit (**Fig.4.3**) was compared by HSPICE PVT and Monta Carlo simulations. In **Fig.4.6** is presented the behavior in time for the reference voltage with the standard autozero architecture (VREF_AZ_V0), and with the improved one (VREF_AZ_V1) at 1.8V for 25°C. In all investigated scenarios (PVT and MC sims), VREF_AZ_V1 is constant in the conversion time domain of the sensor, while VREF_AZ_V0 has a considerable drift over time.

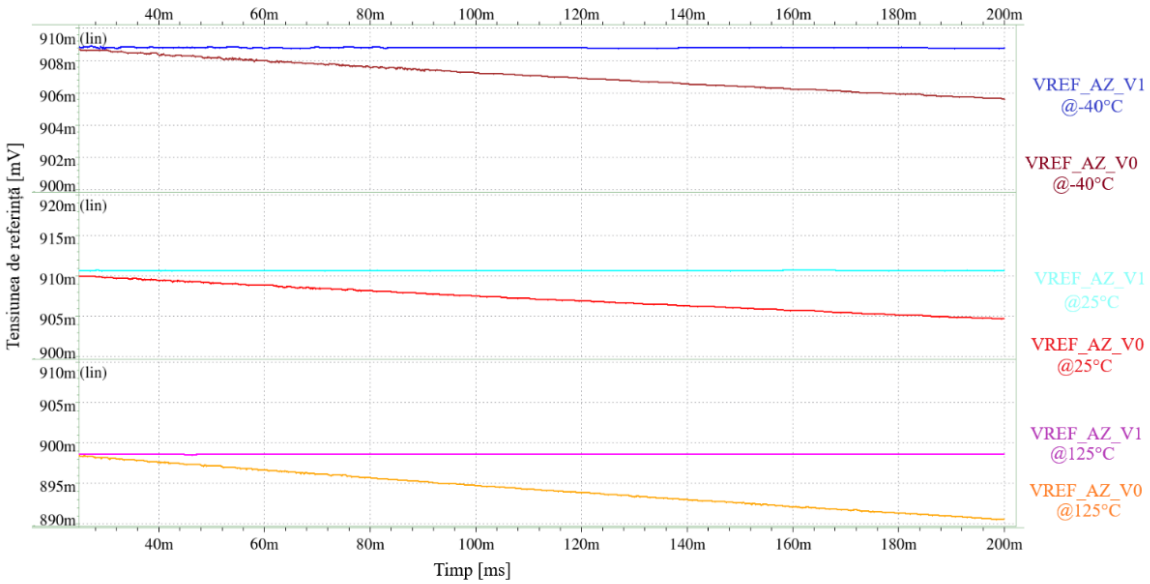


Fig. 4.6 *The behavior of reference voltage the 1.8V*

4.6 DTS I²C experimental results with the improved autozero architecture

The DTS I²C sensor with the improved autozero architecture (**Fig.4.4**) was SI implemented. The circuit was validated by wafer measurements for power supply voltages V_{DD} = 1.8V and test voltages V_{DD_TEST} = 3V and 3.3V at temperatures of 25°C, 50°C and 90°C. In **Fig. 4.7** is shown the behavior of the reference voltage V_{REF_OUT} for 5s at 90°C. V_{REF_OUT} is equal with 930 mV on the entire investigated time. The oscilloscope capture (**Fig. 4.7**) confirms the simulated results (**Fig. 4.6)**, where the reference voltage obtained with the improved autozero architecture is constant over the entire measured time interval.

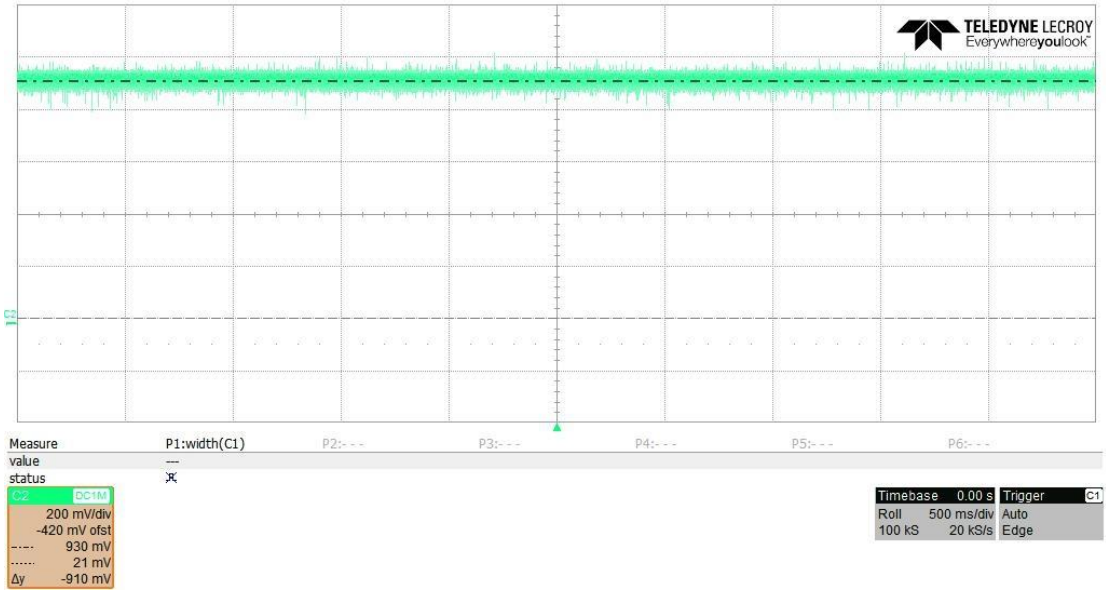


***Fig. 4.7** Oscilloscope capture for V_{REF_OUT} at 3.0 V and 90°C*

Chapter 5

Digital output circuits for DTS I²C in a CMOS EEPROM process

5.1 Introduction

The DTS I²C sensor incorporates a serial interface that enables communication with a CPU. Depending on the communication protocol employed, a dedicated digital output circuit (digital output buffer) is selected. For instance, the Standard, Fast Mode (FM), Fast Mode+ (FM+) and High Speed (HS) I²C interface utilize an open-drain digital output buffer operating at speeds up to 3.4MHz (HS), C_B = 550pF (FM+), I_{OL} = 20mA (Standard).

On the other hand, the I^{2}C Ultra-Fast Mode (UFm) and SPI interface utilize a push pull digital output buffer, allowing operation at higher speeds – up to 10MHz, C_B = 30pF and current loads of +/-3mA. As emerging trends emphasize faster interfaces for communication between a CPU and the sensor, the analysis will focus on push-pull buffers for I2C UFm and SPI, and open-drain output buffers for I^{2}C HS interface.

5.2 The Push-Pull Output Buffers. Standard Implementation

The standard push-pull circuit, depicted in **Fig. 5.1,** was designed in a 0.18µm CMOS EEPROM. Its behavior was investigated using HSPICE simulations across power supply range of 1.6V to 5.6V, temperatures from -40°C to 125°C, f_{IN} = 5MHz and C_L = 30pF. The parameters of the standard push-pull buffers are summarized in **Tabel.5.1**. A maximum propagation delay (t_{pHL}) of 28.1ns is observed at 1.6V, representing ~ 60% of the total transmission data time for the entire I^{2}C UFm interface. Additionally, the SPI interface imposes a maximum data transmission time of 25ns. However, the standard push pull circuit (**Fig.5.1**) cannot operate at 5MHz for the entire power supply range for either of these two interfaces.

For low voltages at 1.6V, the delay introduced only by the response time of the final stage (t_{D_N1}, t_{D_P1}) accounts for half of the total propagation delay (**Tabel.5.1**). Notably, a significant contributor to the high t_{pHL} is the nonoverlap circuit, representing ~ 40% of the propagation delay. Comparatively, the classic push-pull buffer (**Fig.5.1**) at 5.6V offers 4 times lower delay times (**Tabel.5.1**), because most of the component blocks are implemented with HV transistors. These HV devices exhibit a larger response time for LV voltages.

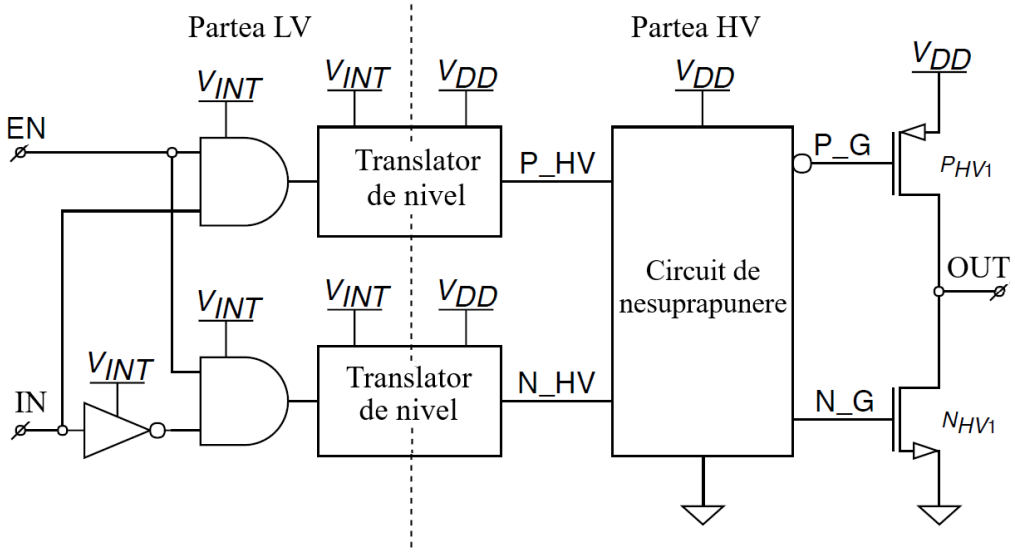


Fig. 5.1 *The electrical schematic of the standard digital output circuit*

Table 5.1 *The parameters of the standard push-pull circuit*

Parameter	**Power Supply Voltage**	**Value**		
		Min	***Typ***	***Max***
t_r [ns]	1.6V	6.2	8.0	9.3
	5.6V	1.2	1.4	1.8
t_f [ns]	1.6V	5.2	6.7	7.5
	5.6V	0.9	1.2	1.5

Parameter	Power Supply Voltage	Value		
		Min	***Typ***	***Max***
t_{pLH} [ns]	1.6V	19.8	25.5	28.1
	5.6V	5.5	6.7	7.5
t_{pHL} [ns]	1.6V	16.8	20.8	24.8
	5.6V	4.4	5.9	6.2
t_{D_N1} [ns]	1.6V	9.8	11.6	13.9
	5.6V	0.96	0.98	1.07
t_{D_P1} [ns]	1.6V	5.3	5.9	7.0
	5.6V	0.6	1.2	1.6
t_{NOV_R} [ns]	1.6V	8.4	9.2	12.3
	5.6V	1.14	1.2	1.6
t_{NOV_F} [ns]	1.6V	4.3	5.2	6.9
	5.6V	0.5	0.6	0.7
I_{DD} @ 5MHz [mA]	1.6V	0.342	0.347	0.356
	5.6V	1.26	1.28	1.31

5.3 The improved architecture of the push-pull circuit

The improved push-pull circuit, illustrated in **Fig.5.2**, introduces a novel architecture by adding a different type of nMOS HV transistor with a lower threshold voltage compared to the one previous used in **Fig.5.1** for N_1 [14] [17]. This modification allows the final nMOS transistor can be controlled with a LV signal, thereby reducing the significant delay associated with HV devices. The same nMOS device is employed for controlling the gate of P_1. Additionally, the nonoverlapping circuit of P_G and N_G is modified for reduce the propagation delay at low power supply voltages.

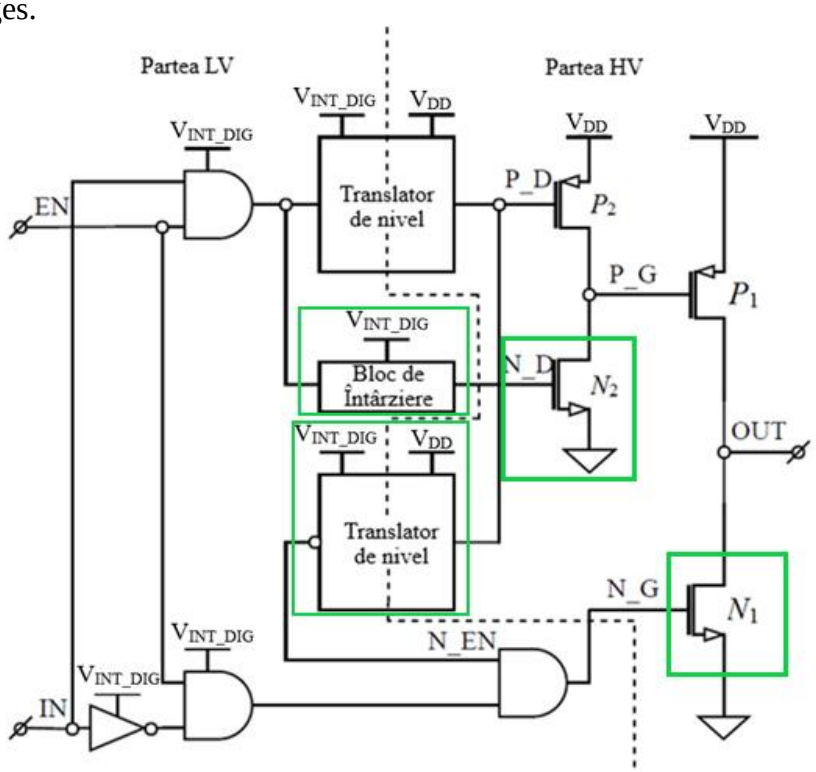


Fig. 5.2 *The electrical schematic of the improved digital output circuit*

The parameters of the improved push-pull circuit are presented in **Table.5.2.** A significant ~ 50% improvement in the propagation delay is observed at 1.6V, making it sufficiently low for acceptance in interfaces such as I^2C UFm and SPI [13]. Furthermore, a 15% reduction in current consumption is achieved due to the majority of LV devices used for the proposed architecture.

Table 5.2 *The parameters of the standard push-pull circuit*

Parameter	**Power Supply Voltage**	**Value**		
		Min	***Typ***	***Max***
t_r [ns]	1.6V	5.7	6.7	8.6
	5.6V	1.4	1.6	1.9
t_f [ns]	1.6V	1	1.2	1.4
	5.6V	1.2	1.4	1.8
t_{PLH} [ns]	1.6V	8.9	11.0	14.2
	5.6V	5.6	6.7	8.5
t_{PHL} [ns]	1.6V	6.9	9.0	12.5
	5.6V	6.2	7.7	10.5
t_{D_N1} [ns]	1.6V	6.4	6.7	7.1
	5.6V	4.5	4.9	5.6
t_{D_P1} [ns]	1.6V	3.7	4.0	4.7
	5.6V	0.7	0.77	0.97
t_{NOV_R} [ns]	1.6V	4.0	4.6	5.8
	5.6V	3.9	4.2	5.1
t_{NOV_F} [ns]	1.6V	2.6	3.1	3.2
	5.6V	4.7	4.9	5.5
I_{DD} @5MHz [mA]	1.6V	0.295	0.297	0.303
	5.6V	1.027	1.031	1.036

5.4 The comparison of the standard and the improved push-pull circuits for I^2C UFm and SPI

I^2C UFm and SPI Interfaces are designed in 0.18µm CMOS EEPROM process [13]. The push-pull circuits presented in **Fig.5.1, 5.2** were compared based on the the data valid time (**$t_{VD,DAT}$**), a critical parameter for data transmission. The PVT simulated results for the two investigated interfaces with the standard push-pull architecture (OUT _V0) and the improved one (OUT _V1) are presented in **Fig.5.4, 5.5**. For each type of interface, a product's parameter was analyzed (PCU9661 for I^2C UFm – **Fig.5.4** and CAT25128, NXH5014 for SPI – **Fig.5.5**). The data valid time with the improved push-pull circuit presented in **Fig.5.2** shows 50% improvement for power supplies below 1.9V compared to the parameter with the classical push pull topology (**Fig.5.4, 5.5**). Furthermore, the performances of the data valid time with the proposed output buffer are better than PCU9661's values for the entire power supply ranges. Also, **$t_{VD,DAT}$** with the improved push pull output circuit shows better performances than the one obtained with CAT25128 and NXH5014 for almost all cases (**Fig.5.4, 5.5**).

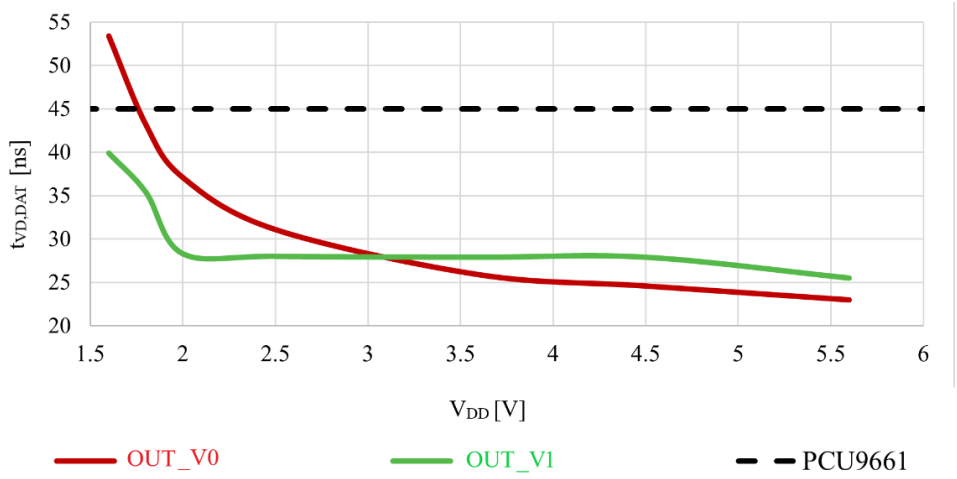


Fig. 5.4 *$t_{VD,DAT}$ for I2C UFm using the investigated push-pull circuits*

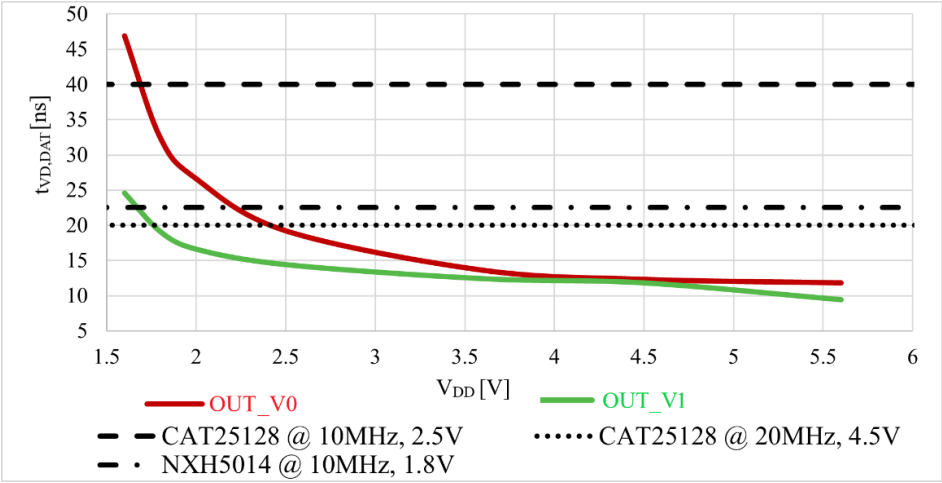


Fig. 5.5 *$t_{VD,DAT}$ for SPI using the investigated push-pull circuits*

5.5 The standard open-drain output circuit

The output circuits with open-drain topology are analyzed for another type of interface: I^2C HS (3.4MHz), targeting fast serial interfaces for digital temperature sensors. The standard open-drain output circuit (**Fig. 5.6**) was designed in a 0.18µm CMOS EEPROM, and its behavior was analyzed using HSPICE simulations for power supply voltages between 1.6V to 5.6V, temperatures ranging from -40°C to 125°C, f_{IN} = 3.4MHz, R_{EXT} = 500Ω and C_L = 100pF. In this topology, the output stage is formed by a transistor with an open drain terminal to which an external resistance (pull-up resistance) is added to V_{DD}. The standard open drain parameters are represented in **Tabel.5.3**. A maximum 120.71ns propagation delay was obtained at 1.6V, which is twice as high as the data valid time imposed by the I^2C HS protocol.

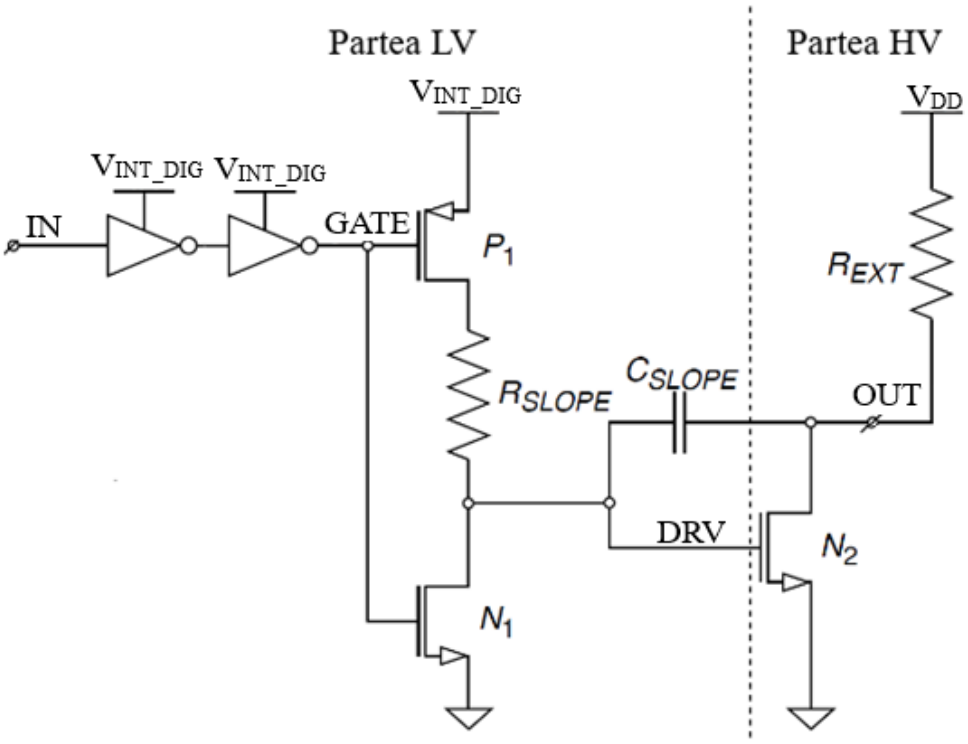


Fig. 5.6 *The electrical schematic of the standard open drain output circuit*

Tabel 5.3 *Standard open drain output circuit's paramaters*

Parameter	Power supply voltage	Value		
		Min	Typ	Max
t_r [ns]	1.6V	111.43	111.72	111.78
	5.6V	110.67	110.78	110.83
t_f [ns]	1.6V	25.03	34.58	56.02
	5.6V	44.16	56	72.07
t_{pLH} [ns]	1.6V	18.74	24.44	36.46
	5.6V	32.27	34.68	39.21
t_{pHL} [ns]	1.6V	40.87	66.61	105.8
	5.6V	66.49	88.39	120.71
I_{VINT_DIG} @ 3.4MHz [µA]	1.6V	3.09	4.3	5.89
	5.6V	3.66	5.08	6.55

5.6 The Improved open-drain output circuit

The novelty in the improved open drain circuit (**Fig. 5.8**) involves the addition of a pMOS transistor P_2 with the purpose of increasing the speed of the output transistor N_2 [18]. The added transistor is controlled by several logic gates, a Trigger Smith and a voltage reference formed by R_{PU} and N_3 transistor. The improved circuit was implemented in 0.18µm CMOS EEPROM and investigated in the same conditions as the standard circuit. The parameters of the proposed circuit are presented in **Tabel.5.4**. A 50% reduction in the propagation delay with the new architecture was achieved for the entire power supply range. Regarding current consumption, 20% increase in values can be observed due to the added devices for a faster output circuit.

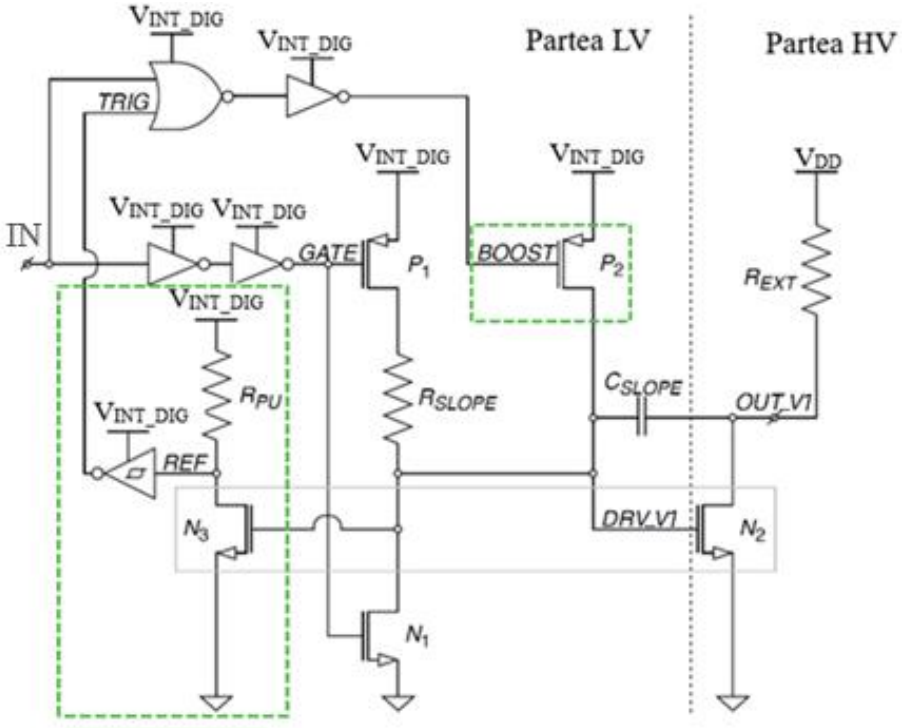


Fig. 5.7 *The electrical schematic of the improved open drain output circuit*

Table 5.4 *The improved parameters of the proposed open drain buffer*

Parameter	Power supply voltage	Value		
		Min	***Typ***	***Max***
t_r [ns]	1.6V	111.07	111.31	111.36
	5.6V	109.96	110.31	110.55
t_f [ns]	1.6V	23.13	34.72	56.02
	5.6V	49.97	56.02	73.60
t_{PLH} [ns]	1.6V	17.81	24.24	36.26
	5.6V	32.27	34.68	39.21
t_{PHL} [ns]	1.6V	6.63	15.5	35.27
	5.6V	37.66	44.64	58.45
avg (i_{VINT_DIG}) @ 3.4MHz [µA]	1.6V	4.90	6.47	8.72
	5.6V	5.81	7.7	10.09

5.7 The comparison of the standard and the improved open-drain circuits for I²C HS

The I²C HS interface was designed in 0.18µm CMOS EEPROM [18]. The open drain circuits presented in **Fig.5.6, 5.7** was compared based on the data hold time ($\mathbf{t_{HD,DAT}}$) – a critical parameter for transmitting data through the interface. PVT simulations in HSPICE for data hold time obtained with the standard open drain buffer (OUT _V0) and the improved one (OUT _V1) are investigated. In **Fig.5.8**. the worst-case parameter with both buffers for supply voltages between 1.6V to 5.6V is presented.

$t_{HD,DAT}$ obtained with the improved open drain (OUT_V1) is twice as low as the parameter obtained with the classical topology (OUT_V0). This improvement is consistently maintained for all investigated supply voltages (**Fig.5.8**). The values obtained for $t_{HD,DAT}$ are compared in **Fig.5.8** with the reported parameter for two commercial products that communicates with I^2C HS: TMP112 [19] and N34TS108 [20]. The propagation delay evaluated with the improved open drain circuit is lower than the ones investigated for the commercial products for the entire power supply range (1.6...5.6V).

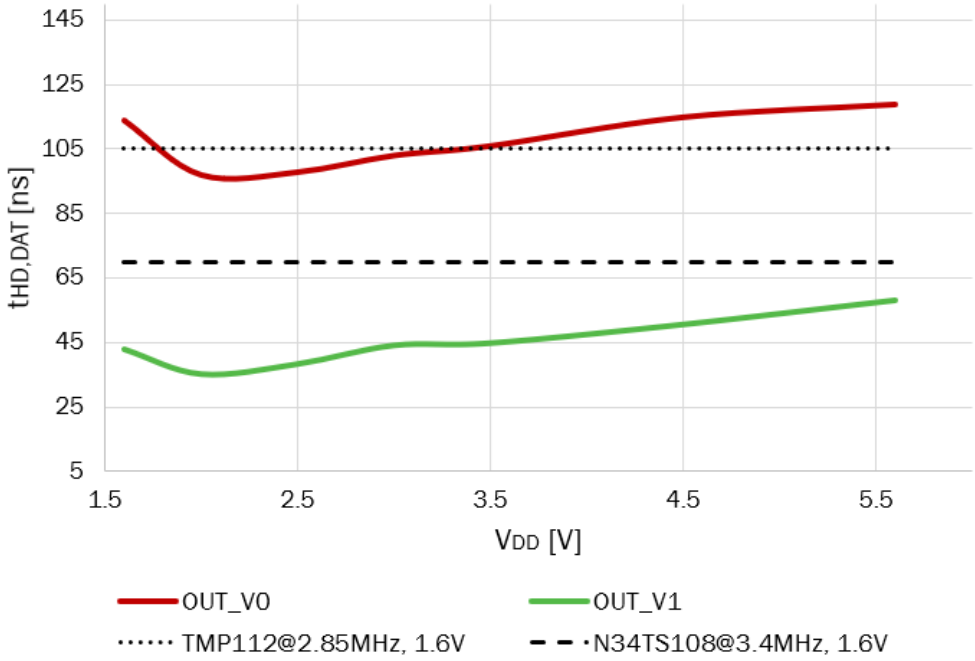


***Fig. 5.8** $t_{HD,DAT}$ for I^2C HS*

5.8 Experimental results of DTS I2C HS with the improved open drain output circuit

The integrated sensor (**3.3**) with the improved open drain I^2C HS interface (**Fig. 5.3**) is implemented in silicon and it was validated by measurements of two encapsulated chips. The parameter $\mathbf{t_{HD,DAT}}$ was measured for temperatures -40°C, 25°C, 90°C, 125°C, power supply voltages from 1.6V to 3.6V and f_{SCL} = 3.4MHz [21]. The investigated data hold time is illustrated in **Fig.5.9**.

The analyzed parameter (**Fig. 5.9)** presents values between 61.18ns and 85.74ns by varying the temperature and the applied voltage. The maximum value is obtained at 1.6V and -40°C, while the minimum value is achieved at 125°C and 1.9V. A bigger variation for the investigated parameter can be seen for low voltages from 1.6V and 1.9V. These values are compared with the simulated data of the sensor with the standard buffer ($\mathbf{t_{HD,DAT\_V0}}$) and the ones obtained with the proposed buffer ($\mathbf{t_{HD,DAT\_V1}}$).

The measurements obtained in **Fig. 5.9** present a 30% improvement than the simulated DTS with the classical open drain topology ($\mathbf{t_{HD,DAT\_V0}}$). Thus, the measured data are ~ 40% greater than the simulated results with the improved architecture ($\mathbf{t_{HD,DAT\_V1}}$). This fact is happened because not only the output circuits add delay on the propagation data line, but also the input circuits of the interface (**IN_SDA**, **IN_SCL** - **Fig.3.3**) contain several HV devices which can determine considerable delays.

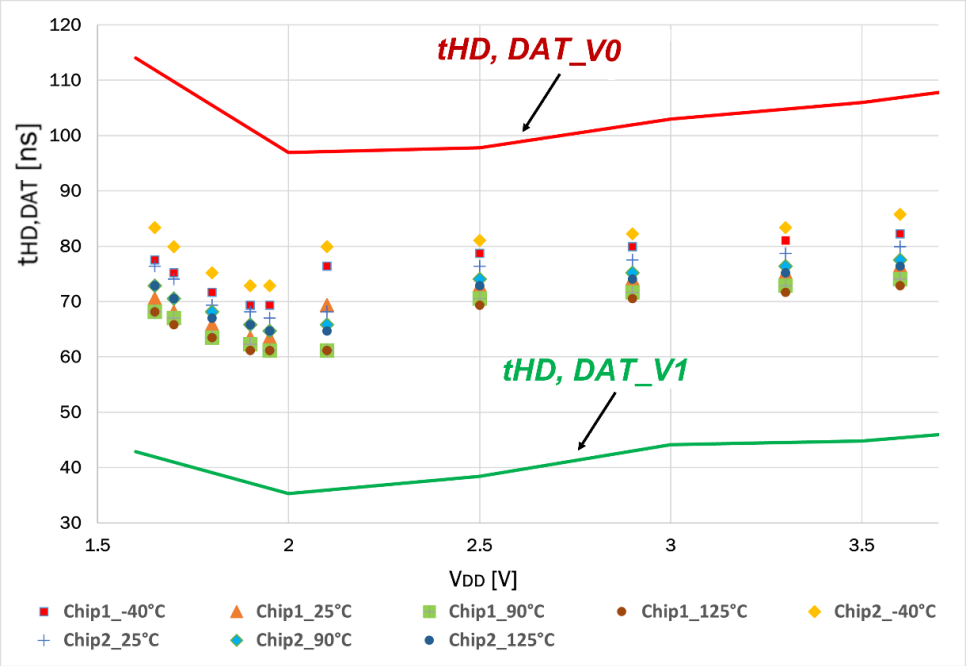


Fig. 5.9 *t_{VD,DAT_HL} – Experimental results VS. PVT Simulations*

Chapter 6

The EEPROM DTS I²C HS sensor in a CMOS EEPROM process

6.1 Introduction

The digital temperature sensor (EEPROM DTS I²C HS) with the improved autozero reference voltage (**Fig.4.4**) and the enhanced open drain I²C HS interface (**Fig.5.7**) was implemented in 0.18µm CMOS EEPROM. For achieve optimal accuracy, trimming circuits for temperature error of the investigated sensor will be analyzed in this chapter. The reference voltage will be adjusted using EEPROM cells to minimum temperature errors for the EEPROM DTS I²C HS. The system with the trimming circuit will be SI implemented and its accuracy will be validated through measurements of several encapsulated chips.

6.2 The Methods for adjusting the temperature error

DTS sensors require an adjustment to achieve the desired performances. Conventional methods involve permanent modification of the circuit using a laser (“laser fuse method”) or altering metal fuses (“metal fuse method”). Additionally, methods using programmable cells one

time (OTP) or EEPROM cells for trimming the part have become more accessible. The use of EEPROM cells for adjusting the sensor offers the advantage of employing increased digital trim codes with a low cost of production.

6.3 The EEPROM trimming circuit for DTS I^{2}C HS

The block schematic of the EEPROM trimming circuit (EEPROM TRIM) for DTS I^{2}C HS is illustrated in **Fig.6.1** [22] [23]. Two EEPROM cells (EEPROM_L and EEPROM_R) are used to obtain a programmable bit. These cells are programmed by a dedicated block with complementary data (PROG EEPROM). Depending on the EEPROM programming, the OUT signal can assume a logic value of 0 or 1 logic.

The advantage of using this type of circuit is the ability to reprogram the cells as required. For adjusting the integrating sensor, 16 EEPROM TRIM and 32 EEPROM cells is employed. Consequently, the trimming signal becomes a digital code of 16 bits.

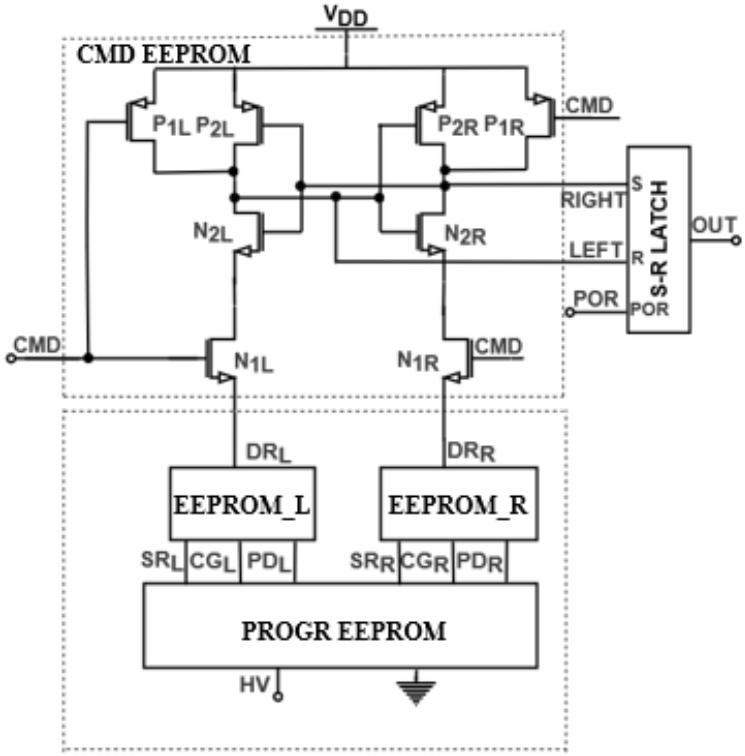


***Fig.6.1** The block schematic of the EEPROM trimming circuit (EEPROM TRIM)*

6.4 The improved architecture of EEPROM DTS I^{2}C HS

The schematic of the proposed sensor EEPROM DTS I^{2}C HS is presented in **Fig.6.2**. The proposed circuit comprises the DTS I^{2}C sensor (**Fig.3.1**) with 16 EEPROM trimming circuits (**Fig. 6.1)**. The integrated temperature detector with I^{2}C High Speed interface contains all the improvements presented in chapters 4 and 5: the voltage reference DTS I^{2}C with the improved autozero circuit (**Fig. 4.3**) and the I^{2}C HS interface with the proposed open drain output architecture (**Fig. 5.7**). Furthermore, the DTS I^{2}C HS contains the EEPROM TRIM block (**Fig.**

6.1) which it is used to adjust REF DTS I2C (**Fig. 4.1**) for obtaining a minimal temperature error for the integrated sensor.

The complete system of EEPROM DTS I^2C HS (**Fig.6.2**) was SI implemented in 0.18µm CMOS EEPROM process [22]. The behavior of the integrated system was validated through tests and measurements at wafer level, as well as measurements of encapsulated chips at various temperatures (-20...125°C) and power supply levels (from 1.7V to 3.6V). The experimental data was then compared with the simulated results.

To adjust the temperature error, the reference REF DTS I^2C is trimmed, achieving different values for the reference current depending on the digital trim code applied (**Fig.6.3(a)**). This process allows for obtaining a correction domain for the temperature (**Fig.6.3(b)**). During testing, the optimal digital trim code is chosen to achieve the desired accuracy of the integrated sensor.

The dependency of the reference current I_{REF} for the sensor EEPROM DTS I^2C HS (**Fig. 6.2**) on the temperature and the optimal digital code applied is investigated in HSPICE simulation as depicted in **Fig.6.3(a)**. I_{REF} can be adjust between 7.5µA and 8.5µA. By using minTRIM (all 16 bits set to 0) and maxTRIM (all 16 bits set to 1) the correction domain of the temperature sensor is obtained (**Fig.6.3(b)**). The EEPROM DTS I^2C HS sensor (**Fig.6.2**) can be adjust between ±30°C (**Fig.6.3(b)**). The selection of the optimal trim to achieve the desired accuracy is performed at the encapsulated chip level.

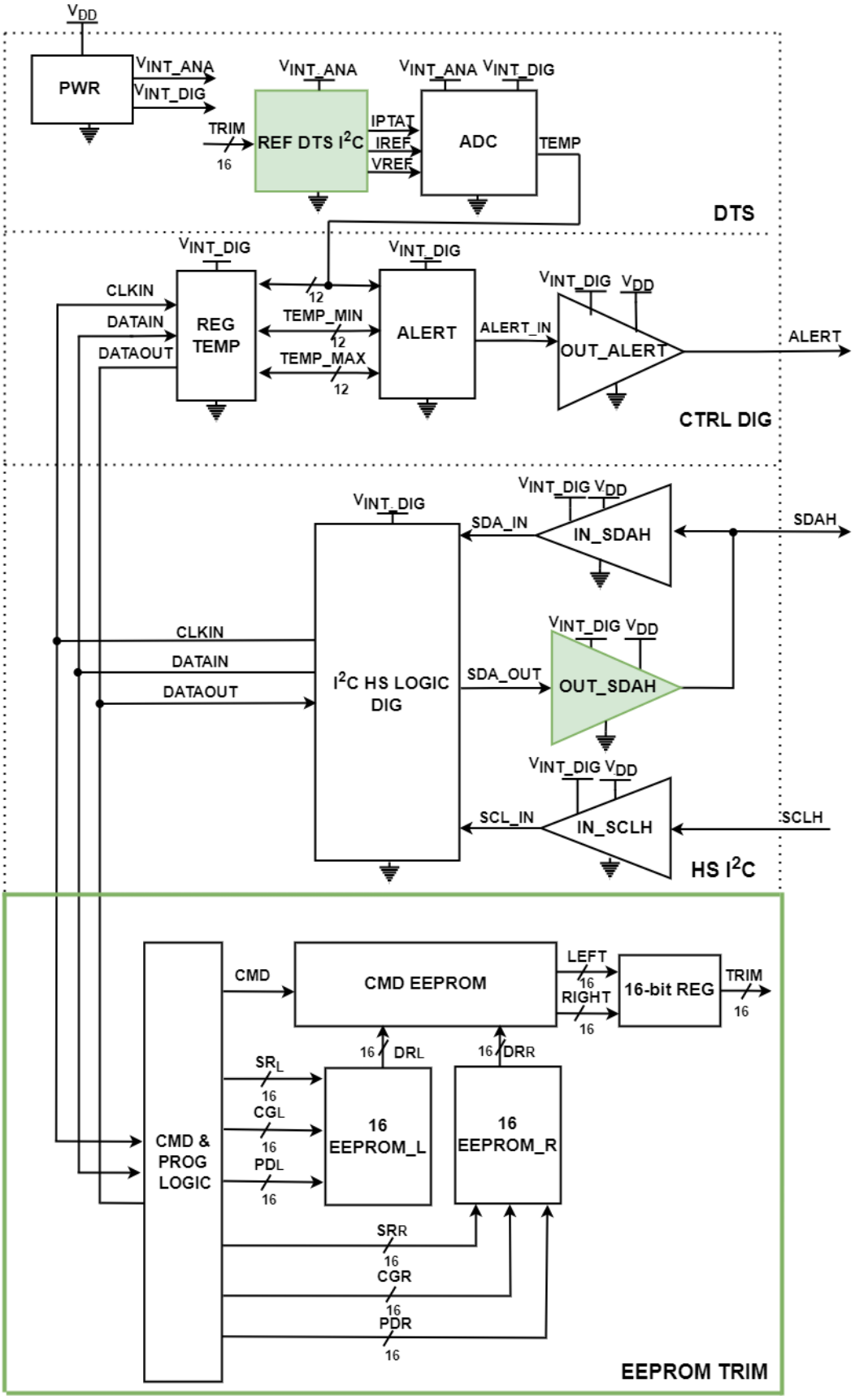
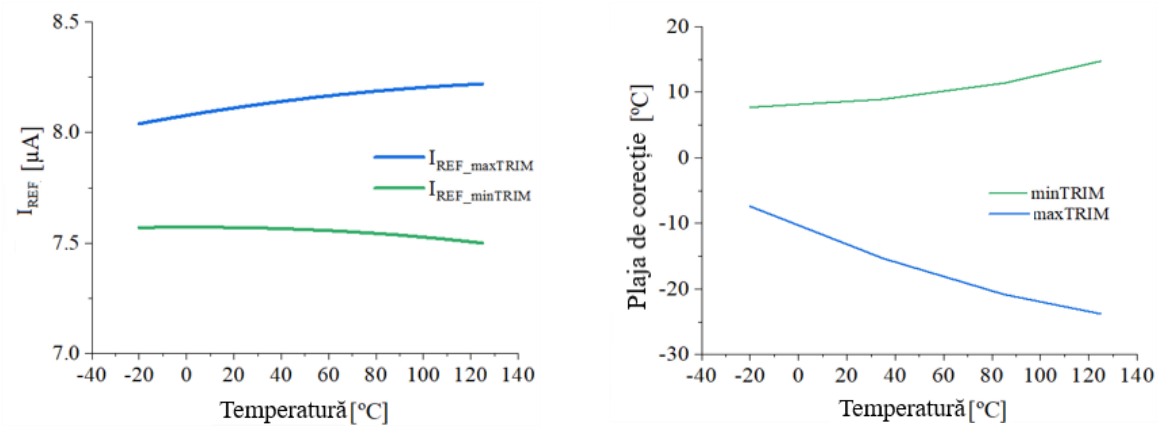


Fig.6.2 *The block schematic of EEPROM DTS I²C HS*



(**a**) (**b**)

Fig.6.3 *(a) I_{REF} vs. TRIM; (b) Correction domain of the temperature*

The EEPROM DTS I^{2}C HS system (**Fig. 6.2**) is adjusted with an optimal digital code in the process of testing for each encapsulated chip. The measured error for 5 EEPROM DTS I^{2}C HS at 1.8V across the entire detected temperature range is illustrated in **Fig. 6.3**. An accuracy of ±1°C is achieved. For majority of tested circuits, the error varies by ±0.5°C in the measured temperature range.

Further investigations were conducted on an additional 20 encapsulated sensors, tested at temperatures between -20…125°C and power supply voltages between 1.7V…1.9V. The measured results show errors within the interval of -1.0°C and+1.56°C (min, max). The mean error at 1.8V across the entire detected temperature range is centered at 0.44°C with a standard deviation of 0.44°C.

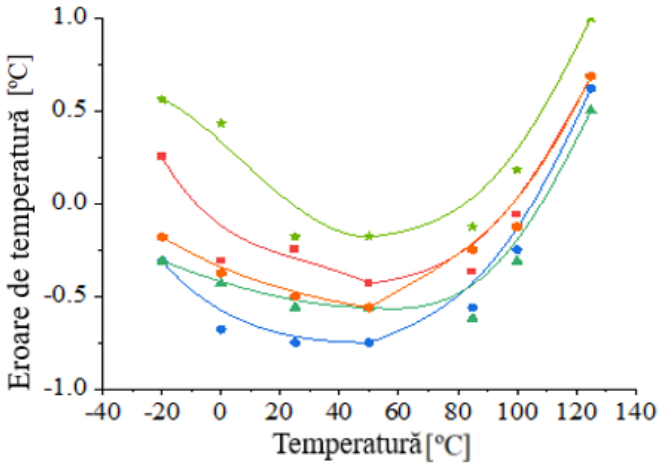


Fig. 6.4 *Measured error of 5 EEPROM DTS I^{2}C HS at 1.8V*

6.5 The comparison of EEPROM DTS I2C HS with integrated sensors from semiconductor's market

The performance of the proposed sensor (**Fig.6.2**) is compared with four families of current digital sensors. The proposed sensor operates at up to 3.4MHz, similar to TMP1075 and N34TS108.The temperature error of the EEPROM DTS I^{2}C HS is ±0.5°C lower than that achieved by N34TS00 and N34TS04. Furthermore, the current consumption of the proposed

sensor is 4 times improved than N34TS00/04. Additionally, the occupied area of the EEPROM DTS I^2C HS is three times lower than N34TS00 and N34TS04.

Table 6.1 *Comparison of EEPROM DTS I^2C HS with four families DTS's products*

Integrated Circuit	**Power supply voltage [V]**	**Detected Temperature range [°C]**	**Temperature Error [°C]**	**Frequency [MHz]**	**Current Consumption [µA]**	**Area consumption [mm^2]**	**Use case**
EEPROM DTS I^2C HS	**1.7…3.6**	**-20…125**	**+1.56/-1.0**	**3.4**	**235**	2.07	DDR4
N34TS00	1.7…1.9	-20…125	± 3	0.4	500	2x3x0.75	DDR4
N34TS04	2.2…5.5	-20…125	± 3	1	1000	2x3x0.75	DDR4
TMP1075	1.6…5.5	-55…125	± 2	3.4	15	1.9	Electronics
N34TS108	1.4…3.6	-40…125	± 1	3.4	6	0.96	Electronics

Chapter 7
Conclusions

7.1 Obtained results

The PhD thesis is dedicated to the digital temperature sensors with integrated serial interface used for DIMM DDR4 memory modules. For this system, new low-power blocks were designed and implemented: the autozero circuit, the open-drain digital output buffer and push-pull output circuit and the EEPROM trimming circuit. The temperature sensor with the serial interface High Speed I^2C and the EEPROM TRIM is implemented in 0.18µm CMOS EEPROM process with low voltage and high voltage transistors. The functionality of the circuit was validated by measurements of encapsulated chips. Also, the performance of the proposed sensor is compared with similar products on the semiconductor's market.

The second chapter offered an overview about several temperature sensors topology and read-out circuits. The targeted parameters of the digital temperature sensor with integrated serial interface were presented, being the most wanted ICs on the semiconductor's market of DIMM DDR4 memory modules.

The third chapter presented the architecture of the digital temperature sensor formed by the detector itself and a read-out temperature circuit, a digital control circuit and a serial interface which it realizes the communication with the digital system.

The fourth chapter is dedicated to the autozero circuit from the componence of the reference voltage. This block serves to eliminate the offset. First, a standard architecture of autozero circuit is investigated by HSPICE simulations in 0.18µm EEPROM CMOS process. The simulations showed a drift over time for the reference voltage as the investigated time increase, as lower the power supply voltage and as the temperature is higher. This behavior has

a negative impact for the functionality of the entire sensor because the reference voltage should be constant in the interval where the analog to digital conversion of the temperature is done (approx. 200ms).

A drift over time can be decisive for evaluating the temperature. Thus, a new architecture for the autozero circuit is proposed to eliminate the phenomenon seen in simulations. The proposed block assures a constant voltage. This behavior was probed by PVT and MC simulations. Furthermore, the voltage reference with the proposed circuit was tested in SI for validate the new architecture of autozero block. Measurements at wafer level was realized for temperatures of 25°C, 50 C and 90°C, power supply voltage of 1.8V, test voltages of 2.7V, 3V, 3.3V for diverse time intervals (200ms and 5s). The oscilloscope captures confirms a constant voltage for the entire detected temperature range and conversion time.

In fifth chapter the output circuits of the serial interfaces (I^2C HS, I^2C UFm, SPI) are investigated. At first, the classical architecture was analyzed. The new trends of developing sensors for DIMMs requires faster and low power interfaces. The I^2C UFm interface operates at frequencies of 5MHz with a capacitive load of 50pF and current load of 3mA. The classical interface of the push-pull digital output buffer was designed and simulated for 1.6...5.6V, -40...125°C. The maximum propagation delay obtained with the classical circuit is 28.1ns, representing more than 25% of the semi period of the targeted frequency. This obtained result can negative influence the correct transmission of the data for the analyzed digital interface. Thus, a new architecture for push-pull topology is proposed to satisfy the demands imposed by the actual faster interfaces. The proposed circuit is analyzed in the same conditions as the classic one. Those two architectures were included in two interfaces: SPI and I^2C UFm. The proposed circuit is 50% faster in both cases.

Also in chapter 5, an open drain output buffer was designed in 0.18µm CMOS EEPROM and it was simulated at 1.6...5.6V, -40...125°C and 3.4MHz (the frequency required for I^2C HS). The maximum response time of the circuit is 130ns, limiting the propagation of the data to 1.7MHz. A new architecture for the open drain is proposed for eliminate the limitations of the classical topology. In the same simulation conditions, the performances of the new circuit are superior by 50%, resulting a maximum time of 58ns.

Moreover, the temperature sensor with the I^2C HS interface which it includes the proposed open drain circuit is SI implemented. The propagation time with the new architecture was measured from 40°C to 125°C and power supply voltages from 1.6V to 3.6V for two encapsulated chips, resulting values between 61.13ns and 85.74ns. Thus, the use of the proposed open drain output circuit for the I^2C HS of the temperature sensor was validated.

The sixth chapter presented the digital temperature sensor with all the proposed improvements in chapters four and five. In plus, the methods for adjusting the digital temperature were investigated to obtain the accuracy required by the application. For memory modules, a ± 2°C temperature error in the detected temperature range of -20…125°C for 1.7V la 3.6V was targeted. The trimming circuit with EEPROM cells was considered the most efficient for the integrated sensor.

The digital temperature sensor with the I2C serial interface and the EEPROM trimming circuit was designed in 0.18µm CMOS EEPROM and was SI implemented. 25 encapsulated circuits were measured at temperatures between -20…125°C and power supply voltages 1.7V…1.9V. A -1.0°C/ +1.56°C accuracy was observed by the experimental data.

Also, in the sixth chapter the proposed sensor was compared with four families of commercial sensors on the semiconductor's market. The proposed EEPROM DTS I2C presents comparable performances with N34TS00 and N34TS04 from the detected temperature and the power supply point of view. The temperature error of EEPROM DTS I2C HS is lower with ±0.5°C than N34TS00 and N34TS04. Furthermore, the current consumption is 4 times less than

the N34TS04 circuit. The spending area of the EEPROM DTS I2C HS is 3 times lower than N34TS00 and N34TS04.

7.2 Original contributions

The presented paper comprises several original contributions, which was disseminated during the research in diverse publications. These includes patents, proceedings of the conferences, scientific journals, and profile events. The following aspects with original character are enlightened:

- Synthesis from literature in the field considering:
  - The market of the digital temperature sensors.
  - The digital temperature sensors with integrated serial interface for DIMM DDR4 memory modules: architectures, parameters, functionality, applications.

- Improved architectures for several internal blocks for the digital temperature sensor:

  - The autozero circuits used in the reference voltage DTS I^2C. This circuit was proposed in a US patent [2].
  - The push-pull circuit for the I^2C Ultra-Fast Mode interface [8], [9]. This proposed circuit was proposed in a US patent [4].
  - The open drain output circuit for I^2C High Speed interface [1], [6], [7].
  - The trimming circuit with EEPROM cells for adjusting the temperature error of the integrated sensor [3], [5].

- SI implementation in a 0.18 µm CMOS EEPROM process of the EEPROM DTS I^2C HS system and of the internal blocks with the new proposed architectures for the digital temperature sensor:

  - The temperature sensor EEPROM DTS I^2C HS with the EEPROM trimming circuit [3].
  - The improved auto-zero circuit implemented with low voltage and high voltage devices for eliminating the drift over time of the reference voltage [2].
  - The improved open drain output circuit for I^2C HS [4], [8], [9].

- Standard, PVT, and Monte Carlo simulations for multiple types of integrated temperature sensor with several serial interfaces and all of the internal blocks of the digital temperature sensor. Several comparisons with the classical circuits from the literature and the improved architectures were analyzed.

- The validation of comparison simulations and measurements for the optimal functionality of the temperature sensor EEPROM DTS I^2C HS and the internal blocks with the improved architectures:
  - Validation of the functionality for the integrated sensor in the -20...125°C detected temperature range, power supplies voltages of 1.6...3.6V and data communication frequency of 3.4MHz [3].
  - Validation of the new autozero circuit in SI by means of the measurements at wafer level for several temperatures and power supply voltages.

- Validation of the I^2C HS interface with the new open drain output circuit in SI. Measurements for several encapsulated circuits for diverse temperatures and power supply voltages was realized [1].
- The validation of the EEPROM DTS I^2C HS system.

- Comparison of EEPROM DTS I^2C HS proposed system with four families of digital temperature sensors with integrated serial interface from the semiconductor's market.

7.3 List of original publications

Below are listed the proper papers with the thematic of the doctoral thesis. In these papers was inserted all the original contributions presented in the above paragraph. This action is indicated by the added references after each contribution. The papers [10] and [11] was published before starting the doctoral program. It contains was helpful for establish the thematic of the doctoral thesis and the directions for development of research.

[1] **A Dragan (Vasile),** A. Negut, A. Enache, I. Hurez, V. Anghel, G. Brezeanu, "*In Focus: Data Hold Time for Temperature Sensors with High Speed I2C Interface*", in **Proceedings of the International Semiconductor Conference (CAS)**, 2023, 11-13 Oct. 2023, BDI, Sinaia, Romania, **IEEE**, DOI: 10.1109/CAS59036.2023.10303655.

[2] **A. Dragan,** A. Enache, A. Negut, A. Tache, "*Auto-Zero Amplifier for Reducing Output Voltage Drift Over Time*", Patent, **US11283419 B2**, Mar.22, 2022.

[3] **A. Dragan (Vasile)**, A. Negut, A. Tache, G. Brezeanu, "*A Digital Improvement – Trimming a Digital Temperature Sensor with EEPROM Reprogramable Fuses"*, **Sensors 2021**, 21(5), 1700, Mar. 2021, Q2 (2023) IF=3.9, ISI, **WOS:000628544800001**, DOI: 10.3390/s21051700.

[4] A. Enache, **A. Dragan**, A. Tache, "*Digital Buffer Circuit*", Patent, **US10707872 B1**, Jul. 7, 2020.

[5] **A. Dragan (Vasile)**, A. Negut, A. Tache, G. Brezeanu, "*A Reprogrammable Fuse with EEcells for trimming a Temperature Sensor"*, **Proceedings of the International Semiconductor Conference (CAS)**, 2020, 07-09 Oct. 2020, Sinaia, Romania, pp. 111-114, ISI, **WOS:000637264600025,** DOI: 10.1109/CAS50358.2020.9268008.

[6] **A. Dragan**, A. Enache, A. Negut, A. Tache, G. Brezeanu, "*An improved digital output buffer for a digital temperature sensor with an I2C high speed interface"*, **Solid State Electronic Letters**, Volume 1, Issue 2, Jul 2019, pp 147-151 (2019), **SCOPUS**, DOI: 10.1016/j.ssel.2020.01.003.

[7] **A. Dragan**, A. Enache, A. Negut, A.M. Tache, G. Brezeanu, *A Fast Response Output Buffer for an I2C High Speed Interface*, **Proceedings of the International Semiconductor Conference (CAS)**, 2019, 09-11 Oct. 2019, Sinaia, Romania, pp. 141-144, ISI, **WOS:000514295300029**, DOI: 10.1109/SMICND.2019.8924012.

[8] **A. Dragan**, A. Enache, A. Negut, A.M. Tache, G. Brezeanu, *An Improved I/O Pin for Serial Communication Interfaces*, **Romanian Journal of Information Science and Technology (ROMJIST)**, Vol.22, no. 2, 2019, pp 158-180, Q2(2023) IF=3.5, ISI, **WOS:000472166600006**.

[9] **A. Dragan**, A. Enache, A. Negut, A.M. Tache, G. Brezeanu, *A High Performance Mixed-Voltage Digital Output Buffer*, **Proceedings of the International Semiconductor Conference (CAS),** Oct. 2018, 10-12 Oct.2018, Sinaia, Romania, pp 179-182, ISI, **WOS:000514386700034,** DOI: 10.1109/SMICND.2018.8539840.

[10] **A. Dragan**, A. Negut, A. Enache, V. Anghel, G. Brezeanu, *Charge retention of a Floating gate Transistor for a Reset Controller*, **Romanian Journal of Information Science and Technology (ROMJIST)**, Vol.21, no. 1, 2018, pp 34-48, ISI, Q2(2023), IF=3.5, **WOS:000433876800003**.

[11] **A. Dragan**, A. Negut, V. Anghel, A. Enache G. Brezeanu, *A matter of isolation — A reset controller using Deep N-Well and floating gate technologies*, **Proceedings of the International Semiconductor Conference (CAS)**, Oct. 2017, 11-14 Oct.2017, Sinaia, Romania, pp 297-300, DOI: 10.1109/SMICND.2017.8101230, ISI, **WOS:000425844500066**.

7.4 Perspectives for further developments

The future research will consider design and SI implementation of the digital temperature sensor with I^3C interface for DDR5 module memory, being the following generation of DDR4. The requirements for this type of sensor involve data communication at 12.5MHz and an ±1°C accuracy for temperatures between -55...150°C and power supply voltages from 1.4V. Also, the functionality of the I^3C interface requires the operation up to 1V power supply voltages, capacitive load of 30 pF and current loads of ±4 mA.

A first step in the development of the integrated sensor with I^3C interface is the push-pull output circuit proposed in this paper, which operates up to 10MHz, 1.6V power supplies, 30pF capacitive load and ±3mA current loads. Furthermore, investigations for testing the push-pull output buffer were started for 1V power supply and 12.5MHz, while the new architecture was proposed in the US patent:

- A. Enache, **A. Dragan**, A. Tache, "*Digital Buffer Circuit*", Patent, US10707872 B1, Jul. 7, 2020.

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